



Promising-ARM/RISC-V: A Simpler and Faster Operational Concurrency Model

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Abstract

For ARMv8 and RISC-V, there are concurrency models in two styles, extensionally equivalent: axiomatic models, expressing the concurrency semantics in terms of global properties of complete executions; and operational models, that compute incrementally. The latter are in an abstract microarchitectural style: they execute each instruction in multiple steps, out-of-order and with explicit branch speculation. This similarity to hardware implementations has been important in developing the models and in establishing confidence, but involves complexity that, for programming and model-checking, one would prefer to avoid.

We present new more abstract operational models for ARMv8 and RISC-V, and an exploration tool based on them. The models compute the allowed concurrency behaviours incrementally based on thread-local conditions and are significantly simpler than the existing operational models: executing instructions in a single step and (with the exception of early writes) in program order, and without branch speculation. We prove the models equivalent to the existing ARMv8 and RISC-V axiomatic models in Coq. The exploration tool is the first such tool for ARMv8 and RISC-V fast enough for exhaustively checking the concurrency behaviour of a number of interesting examples. We demonstrate using the tool for checking several standard concurrent datastructure

and lock implementations, and for interactively stepping through model-allowed executions for debugging.

CCS Concepts • Theory of computation → Concurrency; Operational semantics; • Computer systems organization → Architectures; • Software and its engineering → Model checking; Concurrent programming languages; Assembly languages.

Keywords Relaxed Memory Models, Operational Semantics, ARM, RISC-V

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1 Introduction

Writing relaxed-memory concurrent software is notoriously hard. To make matters worse, testing alone cannot give high confidence: the behaviour is highly non-deterministic and certain relaxed behaviours are only observed very rarely, e.g. only once in thousands or millions of executions, sometimes only on particular hardware, sometimes not currently observable at all but allowed by the specification (and so perhaps exhibited with future compiler generations or hardware).

Therefore, precise semantics of the concurrency behaviour and tool support for checking software correctness are highly desirable. More specifically, to safely write such software — typically concurrency library implementations — it is useful to have (i) a clear and precise semantics, ideally helping programmers avoid most bugs in the first place, (ii) exhaustive exploration tools, to find concurrency bugs or show their absence in bounded executions, and (iii) interactive exploration tools, helping to pin down the source of unexpected behaviours of the program.

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While such libraries are mostly written in higher-level languages such as C/C++, semantics and tool support at the assembly level offer several benefits. First, after extensive past research, hardware concurrency models are quite well-understood. For higher-level languages such as C/C++ [16] only non-atomic accesses and the sequential consistency and release/acquire fragments are well-understood. High-performance algorithms, however, also involve relaxed ‘atomics’ and ‘consume’ atomics, for which there still is not an accepted high-level language semantics [15, 27, 29, 38]. Hence, in practice programmers often write code that does not follow the C/C++ concurrency model, relying instead on the compiled code to provide stronger guarantees, e.g. Linux has its own memory model [9, 25]. For example, in C/C++, often weakening ‘consume’ or ‘acquire’ loads to ‘relaxed’ loads, though unsound in the source language, generates more efficient code that behaves correctly under the hardware memory model. Second (and related), in many cases concurrency libraries include hand-written assembly modules or inline assembly, optimised for performance on particular hardware (requiring a clear understanding of the assembly semantics). Third, the compiler need not be trusted because even compiler-introduced bugs can be detected. Fourth, such tools apply for any source language or memory model: e.g. C, C++, Rust, or Linux.

Such assembly tools can, for instance, effectively be used in the following scenario of a code base with custom concurrency libraries: the library functions are separately compiled to assembly, debugged and exhaustively checked (up to some bounds) by the exploration tools, and then linked at the assembly level with client software of the remaining code base (in turn perhaps checked/verified using source level tools).

In this paper we present a semantics and tools aiming to address these goals for the widely used ARMv8 processor architecture [12], that has recently moved to a multicopy-atomic semantics [20, 39], and for RISC-V, whose community has recently ratified a very similar memory model [42]. ARMv8 and RISC-V have relaxed memory models that allow the effects of various processor optimisations to become observable to the programmer: instructions execute out-of-order and speculatively (past unresolved conditional or computed branches), speculative writes can be forwarded to program-order-later reads, processors have store queues and caches to speed up memory accesses, etc. At the same time, the architectures give guarantees of coherence, ordering resulting from dependencies and memory barriers, and atomicity of load/store exclusive instructions. The resulting memory models are subtle, and a clear semantics and tool support are particularly valuable.

For ARMv8-A and RISC-V there are two existing styles of semantics and associated tools: axiomatic and operational, with the latter in an abstract microarchitectural style.

The axiomatic model for ARMv8-A [12, 20, 39] is incorporated by the architecture text; it is formalised by Deacon

in herd [11]. The RISC-V model, recently defined by the RISC-V Memory Model Task Group (chaired by Lustig), is similar, and is formalised both in Alloy [26] and in herd. These axiomatic models describe the semantics by directly stating properties of the legal executions, as axioms about candidate executions. This makes for abstract and concise definitions. But they only specify global properties of completed executions and do not compute the legal outcomes incrementally. We want to support stepping through executions for debugging. Moreover, herd only supports a few instructions, without a substantial instruction-set architecture (ISA) model, and the Alloy model is a pure memory model; it cannot run machine instructions.

The existing operational models for ARMv8 and RISC-V are variants of the Flat operational model, by Pulte, Flur, et al. [39]. Flat computes the possible executions of a concurrent program incrementally, based on the legal traces from the initial state, where the model transitions enabled in a given state are subject to thread-local conditions. It features substantial ISA models for ARM and RISC-V. Moreover it is integrated into the rmem tool [22, 23, 39–41] that supports exhaustive and interactive exploration, a web user interface, debugging facilities, etc. The biggest example exhaustively checked with Flat so far is a spinlock example from the Linux kernel. The model has an abstract micro-architectural flavour. This strengthens confidence in the model, and was important in developing the model in discussion with hardware architects. However, it makes the model complex. It enables but also requires a programmer to think in terms of hardware mechanisms: the model executes instructions in multiple steps (per instruction) and out-of-order; it has explicit branch speculation and sometimes needs to restart instructions to repair mis-speculation.

In this paper we develop a new operational model, PROMISING-ARM/RISC-V, and an interactive and exhaustive exploration tool based on it, inspired by the Promising semantics for C11 of Kang et al. [29]. Our model has the abstractness of the axiomatic models but computes locally and incrementally, making it a simpler operational model. In contrast to Flat, this model executes an instruction in a single step and – except early writes – in order, and does not speculate branches. The exploration tool integrates models for large parts of the user-mode ARMv8 [22] and RISC-V [13] ISAs written in Sail [13, 24] (the same as those used by Flat). This provides a significant advantage over the axiomatic models that do not include a substantial ISA model. By integrating into rmem, our model also benefits from the infrastructure it offers, including a web UI, debugging facilities, e.g. the ability to set breakpoints, show DWARF debugging information for compiled code, etc. Even without applying any model checking techniques, our model is the first such tool for ARMv8 or RISC-V with sufficient performance for exhaustively checking several loop-bounded standard concurrent datastructure examples. We also formalise the

model for a small idealised ISA and prove it equivalent to the ARMv8/RISC-V axiomatic models for finite executions, in Coq. To summarise, the contributions are:

- PROMISING-ARM/RISC-V, a simpler and more abstract operational model, executing instructions in program order, not out-of-order and not speculatively (§4, §5).
- A Coq proof of equivalence with the ARMv8 and RISC-V axiomatic models for a small idealised ISA (§6).
- An interactive and exhaustive exploration tool for ARMv8 and RISC-V user-mode assembly programs (§7).
- A demonstration of the tool for several concurrent data-structures, written in C++ and Rust, compiled with GCC or rustc, including the Chase-Lev deque, Michael-Scott queue, and Treiber stack (§8). We demonstrate using the tool also in checking aggressively relaxed programs that are unsound in the source memory model but sound in ARMv8/RISC-V.

For the supplementary material, see [2].

Caveats We do not yet model mixed-size accesses (Flat does), since their architecturally intended semantics is still being clarified for ARM and RISC-V. We expect we can cover them by handling certain memory accesses byte-wise and with a more fine-grained register dependency handling, analogously to Flat. We do not yet model read-modify-write instructions that we expect to work analogously to load/store exclusive instructions that we do cover. Like Flat, we only handle user-mode non-vector non-floating-point instructions, no systems features or supervisor mode. While in ARMv8 and RISC-V syntactic dependencies enforce ordering, ARM store exclusives are an exception. As a result, like Flat [39], the ARM model can deadlock (but is nonetheless equivalent to the axiomatic model). The RISC-V model has no such deadlocks (again, like Flat), see §4.3 for details.

2 Overview

Our model builds on the work for the C/C++ Promising semantics [29], but has a simpler memory semantics – enabled by the multicopy atomicity and the simpler notion of dependencies in ARMv8/RISC-V – and a new uniform treatment of the dependencies and ordering using timestamps. We now show the main ideas of our model, highlighting the benefits over Flat, and show a key property of the model that allows reducing non-determinism by enumerating the possible final memory states without interleaving reads.

Out-of-order Reads We first show how our model explains the effects of out-of-order reads though executing them in order. Consider the following example (for presentation using a simple calculus); assume every location is initialized to 0. Here Thread 1 (left) writes 37 to x and 42 to y . The stores are kept in order by a strong barrier `dmb.sy`. Thread 2 (right) reads y . If the value read is 42 it reads x ,

otherwise it executes the instructions from g . Despite e introducing a *control dependency* from d to f , ARMv8/RISC-V allow executing f before d , due to branch speculation, and hence the outcome where d reads 42 and f the initial value $x = 0$.

(a) store [x] 37;	(d) r ₀ := load [y]; // 42
(b) dmb.sy;	(e) if (r ₀ = 42)
(c) store [y] 42	(f) r ₂ := load [x] // 0
	(g) else...

Following the mechanisms of micro-architecture, Flat allows this execution by branch speculation. In the initial state, Thread 2 can speculatively fetch and execute either branch of the conditional. Fetching the “then” part before the branch condition is resolved (before a and c are propagated) allows f to read the initial write $x = 0$. Once a and c are propagated, d reads from c and resolves the conditional branch. Since the speculation was correct, f can finish, resulting in the example outcome. Instead of fetching f , Thread 2 could have also fetched the “else” branch, in which case, after reading $y = 42$, Thread 2 would have detected the mis-speculation and discarded any already-executed instructions of that branch.

In contrast, our model *executes loads in order*. It records the full history of writes propagated so far and allows loads to read old values. The above execution is allowed as follows. Executing a , b , and c results in memory $[0 : \langle x := y := 0 \rangle; 1 : \langle x := 37 \rangle; 2 : \langle y := 42 \rangle]$. Here 0 to 2 are *timestamps*, list indices in memory. Then we execute Thread 2 sequentially: d can read any write to y in memory, either $\langle y := 0 \rangle$ or $\langle y := 42 \rangle$. After reading the latter, e takes the “if” branch. Now f can also read either write to x , $\langle x := 0 \rangle$ or $\langle x := 37 \rangle$. This treatment of loads, executing them in program order, leads to a simpler model: simplifying the dependency handling and removing the need to speculate branches and repair incorrect speculation. Moreover, it reduces non-determinism: resulting from the out-of-order execution of reads, and the speculative exploration of possible branch targets – if e was a computed branch, Flat would have to allow fetching *any code location* as a possible successor instruction of e .

Ordering Memory Accesses with Views Changing f in the previous example to $r_2 := \text{load}[x + r_0 - r_0]$ makes f *address-dependent* on d and prevents executing f before d . In the Flat model the dependency prevents executing f early since the register values involved in computing the location of f are not available until d is done. In our model this is handled with *views*. A view records a timestamp of a memory write to capture some ordering requirement. After executing a to c , memory is $[0 : \langle x := y := 0 \rangle; 1 : \langle x := 37 \rangle; 2 : \langle y := 42 \rangle]$, as before. When d reads $\langle y := 42 \rangle$ it annotates register r_0 with c 's timestamp 2. Since f depends on r_0 , this constrains f and prevents reading $x = 0$, which is “out-of-date” at time 2, due to the previous write $\langle x := 37 \rangle$ at timestamp 1.

Instantaneous Instruction Execution In the next example, PPOCA [41], the instructions i and j after e write and read z , and f address-depends on j . Assume d reads 42 and j reads from i . In ARMv8 and RISC-V, control dependencies prevent early execution of writes, and so i cannot propagate to memory before d . Even though f depends on j , which reads from i , f can execute before d , and hence the outcome where f reads $x = 0$ is allowed, because i can forward to j (without i propagating). In Flat this is as follows: as before, Thread 2 speculatively executes the “then” branch; i cannot propagate yet, because e is unresolved; however, i can execute some *intra-instruction* steps and determine its location z and value 51 (in the real ISA this involves several register reads and arithmetic). In this half-executed state i can forward its value 51 to j , resolving f ’s location, and allowing it to read $x = 0$.

(a) store [x] 37;	(d) $r_0 := \text{load } [y]; // 42$
(b) dmb.sy;	(e) if ($r_0 = 42$)
(c) store [y] 42	(i) store [z] 51;
	(j) $r_1 := \text{load } [z]; // 51$
	(f) $r_2 := \text{load } [x + (r_1 - r_1)] // 0$
	(g) else ...

In our model *all instructions execute instantaneously*, and write forwarding is instead explained by views: a read normally receives a view including the view of the write it read from; if it reads from a write by its own thread, however, it acquires a smaller view. Here, after executing a to c the memory is as shown before; when d reads $y := 42$ it annotates r_0 with timestamp 2; due to the control dependency on r_0 , i must write to memory at a timestamp greater than 2 (as explained later). But when j reads from i it can acquire a smaller view, 0, since it is reading from a write by its own thread. Hence r_1 also has view 0 and f can read $x = 0$ from the write history. Executing each instruction in a single step significantly simplifies the model over Flat: conceptually, and by reducing the transitions and rules of the model.

Out-of-order Writes In the final example, Thread 1 reads x and writes y ; Thread 2 reads y and writes what it read to x . The outcome where a and c read non-zero values is allowed, as b can execute early. And that is how Flat allows it.

(a) $r_0 := \text{load } [x]; // 37$	(c) $r_0 := \text{load } [y]; // 37$
(b) store [y] 37	(d) store [x] r_0

In our model, this is explained using *promises*. In a given state S , if a thread could take multiple steps from S sequentially (with no steps by other threads) and produce a write w , then the thread is allowed to promise w in S . A promise binds the promising thread to later *fulfil* the promise. Here, Thread 1 can promise $y := 37$ in the initial state, since executing sequentially it could read $x = 0$ (with a) and write $y := 37$ (with b). The promise yields memory $[0 : \langle x := y := 0 \rangle; 1 : \langle y := 37 \rangle]$. Now c can read $y = 37$ and d write $x := 37$. Finally, a can read $x := 37$, and Thread 1

$p ::= s_1 \parallel \dots \parallel s_n$	<i>program</i>
$s \in \text{St} ::=$	<i>statement</i>
skip $s_1; s_2$ if (e) $s_1 s_2$ while (e) s	<i>control statements</i>
$r := e$	<i>assignment</i>
$r := \text{load}_{xcl, rk} [e]$	<i>load</i>
$r_{succ} := \text{store}_{xcl, wk} [e_1] e_2$	<i>store</i>
dmb.sy dmb.st dmb.ld isb	<i>ARM barriers</i>
fence $_{K_1, K_2}$ fence.tso	<i>RISC-V barriers</i>
$r \in \text{Reg} = \mathbb{N}$	<i>register</i>
$op \in \text{O} ::= + \mid - \mid \dots$	<i>arithmetic ops.</i>
$e \in \text{Expr} ::= v \mid r \mid (e_1 \text{ op } e_2)$	<i>pure expression</i>
$xcl \in \mathbb{B} ::= \text{true} \mid \text{false}$	<i>exclusive or not</i>
$rk \in \text{RK} ::= \text{pln} \mid \text{wacq} \mid \text{acq}$	<i>read kind</i>
$wk \in \text{WK} ::= \text{pln} \mid \text{wrel} \mid \text{rel}$	<i>write kind</i>
$K \in \text{FK} ::= \text{R} \mid \text{W} \mid \text{RW}$	<i>RISC-V fence kind</i>

Figure 1. The language

can execute b and fulfil the promise $y := 37$. In contrast, due to the data dependency, in the initial state Thread 2 cannot promise $x := 37$: executing sequentially, c must read $y = 0$, so d would write $x := 0$.

As detailed later, dependencies also constrain promises in another way. When a thread promises a write at timestamp t , it is later required to fulfil the promise with a view smaller than t , effectively preventing writes from being promised “too early”, using views.

Writes First The example also allows us to illustrate the key idea for reducing the combinatorial problem of exhaustive enumeration. Naively, exhaustive execution would mean checking all interleavings of the reads and writes/promises. However, in our model for every legal trace there exists an equivalent one in which all promises are done first: for example, for the trace “ a (reading 0), c (reading 0), b , d ” the same outcome can be reached as follows: promise $y := 37$ (Thread 1), promise $x := 0$ (Thread 2), read $x = 0$ with a , read $y = 0$ with c . Due to this property, the model can enumerate all final memory states by exploring only the interleavings of write transitions, without interleaving reads.

We now define the sequential calculus and informally explain the model, before giving the precise definition.

3 Language

To focus on the concurrency aspects we consider the small imperative language of Fig. 1; the executable tool of §7 handles user-mode parts of the real ARMv8 and RISC-V ISAs. Statements include loads, stores, barriers, register assignment, sequential composition, conditionals, and loops. Statements operate on registers, of which we assume we have an infinite supply. A load or store is annotated with (1) a boolean indicating whether it is an exclusive access, and (2) a read or write kind, respectively indicating whether it is a plain access or has special acquire or release ordering. A store writes a bit to a register indicating success or failure. Only store exclusives can fail, non-exclusive stores always

succeed, but for uniformity of the syntax and the rules, non-exclusive stores also write the success bit, to an otherwise unused register, that we omit in the syntax. Following the ARM ISA, success is indicated by 0 (here called v_{succ}), and failure by 1 (v_{fail}). Whenever a load or store command is not annotated with a memory kind, we mean plain loads and stores; whenever not annotated to be exclusive, we assume it is non-exclusive. So $r := \text{load } [e]$ is a plain, non-exclusive load, and $\text{store } [e_1] e_2$ is a plain, non-exclusive store.¹ We treat ‘(if (e) s_1 s_2); s_3 ’ as equivalent to ‘if (e) (s_1 ; s_3) (s_2 ; s_3)’ (parenthesising for clarity): control flow is not delimited in assembly programs, and so in our language the instructions in s_3 are control-dependent on expression e . (This matters for the ordering from control dependencies.) As usual, the executable model bounds loops.

4 PROMISING-ARM/RISC-V, Informally

For presentation purposes, we use ARMv8 terminology for barriers: `dmb.sy` for full barriers, etc. We describe the semantics for programs with only plain loads and stores and full barriers. The remaining semantics is a natural extension to the model, detailed in §A of the supplementary material. We first explain the out-of-order execution of loads and how views constrain them in the *view semantics*. We then illustrate how the *promising semantics* extends it to account for the out-of-order execution of stores. Finally, we describe how certification avoids executions with unfulfilled promises.

4.1 View Semantics

The view semantics underlying our model explains the effects of the out-of-order execution of reads – while executing programs in order – by recording the full write propagation history and allowing reading from older writes, not just the last same-address write [31]. The model state $\langle \vec{T}, M \rangle$ comprises the thread pool \vec{T} and the memory M , where \vec{T} maps each thread identifier tid to a statement (of type St), and a thread state, consisting of a register state and more components that we introduce as we proceed. We call a *thread* the pair of a statement and a thread state. We do not model dynamic thread creation; hence, the model transitions do not change the domain of the thread pool. (For reference, §5 has the formal definition of types and rules.)

Memory Memory is a list of writes, in the order they were propagated. A write (message) w , written $\langle x := v \rangle_{tid}$, records the location $w.\text{loc} = x$, value $w.\text{val} = v$, and originating thread identifier $w.\text{tid} = tid$. Initially, memory is the empty list $[]$, which we treat as holding an initial value 0 for all locations. Executing a store generates a write that is appended at the end of memory.

¹RISC-V has a load-reserve acquire-release and store-conditional acquire-release: instructions with (strong) acquire and release ordering combined. For simplicity of the presentation we omit this, but the executable model handles it. We plan on adding this to the Coq formalisation as well.

Consider the following Message Passing (MP) example test, with instruction names $a - e$, and comments added for presentation; to easily distinguish, values are written in blue, thread identifiers brown, and (later) timestamps green. In this test, Thread 1 writes 37 to memory location x , and, after a strong `dmb.sy` barrier, writes 42 to y ; Thread 2 reads y and then x . To focus on the out-of-order execution of loads, we inserted the barrier b between a and c to prevent their reordering. The execution of interest here is that where Thread 2 reads $y = 42$, and then the initial value $x = 0$. This is allowed in ARMv8/RISC-V because the (independent) loads on Thread 2 are allowed to execute out of order.

$$\begin{array}{l} (a) \text{ store } [x] \text{ 37;} \\ (b) \text{ dmb.sy;} \\ (c) \text{ store } [y] \text{ 42} \end{array} \parallel \begin{array}{l} (d) r_1 := \text{load } [y]; \text{ // 42} \\ (e) r_2 := \text{load } [x] \text{ // 0} \end{array}$$

$$r_1 = 42 \wedge r_2 = 0 \text{ allowed}$$

In our model, executing a, b, c leads to the following transitions (b does not change memory):

$$\begin{aligned} \langle \vec{T}, [] \rangle &\stackrel{(a)}{\Rightarrow} \langle \vec{T}', [\langle x := 37 \rangle_1] \rangle \stackrel{(b)}{\Rightarrow} \langle \vec{T}'', [\langle x := 37 \rangle_1] \rangle \\ &\stackrel{(c)}{\Rightarrow} \langle \vec{T}''', [\langle x := 37 \rangle_1; \langle y := 42 \rangle_1] \rangle \end{aligned}$$

Now d can read $y = 42$. Then, since loads can read not only from the last same-address write but also older writes in memory or the initial state, e can read the initial $x = 0$.

Views Memory barriers restore stronger ordering. Placing a `dmb.sy` barrier between the loads of Thread 2 orders them and prevents the behaviour where the load of x reads 0 after d reads 42. Our model handles this ordering using *views*:

R1 A timestamp $t \in \mathbb{T} = \mathbb{N}$ is a natural number index of a write in the message history or 0, where list indices for memory start from 1 and timestamp 0 indicates the initial writes. A view $v \in \mathbb{V} = \mathbb{T}$ is simply a timestamp, indicating that the write at position v and its predecessors in the message history have been “seen”.

Before executing a load or store i , its *pre-view* is computed. The pre-view captures the dependencies and ordering requirements constraining the execution of i . For loads this constrains the values it can read from, for a store (in the later promising semantics) how “early” its write can be promised.

R2 A view constrains loads: a thread can read from the most recent and older writes, but no older than the view allows – it must not read from writes overwritten by newer “seen” same-address writes.

After executing i , its *post-view* is computed. It captures the constraints i imposes on instructions ordered with i .

R3 The post-view of a load is the maximum of its pre-view and the *read-view*. In the examples we consider first, the read-view is simply the timestamp of the write the load reads from; we later refine this to handle *forwarding*. The post-view of a store is the timestamp of its write message (which is always strictly greater than its pre-view).

We gradually introduce how the pre-view of loads and stores is computed.

Memory Barriers Returning to the example, we model the effects of memory barriers using views:

- R4** Each thread state maintains views $v_{rOld}, v_{wOld}, v_{rNew}, v_{wNew} : \mathbb{V}$. Initially, all views are 0.
- R5** v_{rOld} and v_{wOld} , respectively, are the maximal post-view of all loads and stores executed so far by the thread.
- R6** v_{rNew} and v_{wNew} , respectively, contribute to the pre-view of all future loads and stores.
- R7** `dmb.sy` updates both v_{rNew} and v_{wNew} to the maximum of v_{rOld} and v_{wOld} : all future loads and stores program-order-after the barrier are constrained by the post-views of those program-order-before the barrier.

Intuitively, `dmb.sy` orders loads and stores before it with those after it; it is the strongest form of barrier. Other barriers update these two views in a similar but weaker way.

$$\begin{array}{l} (a) \text{ store } [x] \text{ 37; } \\ (b) \text{ dmb.sy; } \\ (c) \text{ store } [y] \text{ 42 } \end{array} \parallel \begin{array}{l} (d) r_1 := \text{load } [y]; \text{ // 42 } \\ (e) \text{ dmb.sy; } \\ (f) r_2 := \text{load } [x] \text{ // 0 } \end{array}$$

$r_1 = 42 \wedge r_2 = 0$ forbidden

In the example, after executing a, b, c , the memory is $[1: \langle x := 37 \rangle_1; 2: \langle y := 42 \rangle_1]$, with timestamps 1 and 2 shown explicitly for presentation. Now, if Thread 2 reads 42, d 's post-view is 2. This is recorded in v_{rOld} . Executing e includes v_{rOld} into v_{rNew} and v_{wNew} : (just showing Thread 2)

$$\begin{array}{l} \langle v_{rOld} = 0, v_{rNew} = 0, \dots \rangle \\ \xRightarrow{(d)} \langle v_{rOld} = 2, v_{rNew} = 0, \dots \rangle \\ \xRightarrow{(e)} \langle v_{rOld} = 2, v_{rNew} = 2, \dots \rangle \end{array}$$

When executing f in the resulting state, f is constrained by a pre-view that includes $v_{rNew} = 2$. Since $\langle x := 37 \rangle_1$ is seen with view 2, f must not read from a write older than that.

While `dmb.sy` provides strong ordering, it comes at a performance cost. Concurrent ARM programs also rely on ordering resulting from dataflow dependencies.

Address Dependencies The next example replaces the `dmb.sy` between the loads of Thread 2 with a *syntactic* address dependency from the first load (d) to the second (e). Register r_1 holding the return value of d is used to compute the address “ $x + (r_1 - r_1)$ ” of load e , which is enough to order d before e , even though the value does not depend on what d read. Similarly to the `dmb.sy`, the ordering from the syntactic dependency means that if d reads 42, then e must read 37.

$$\begin{array}{l} (a) \text{ store } [x] \text{ 37; } \\ (b) \text{ dmb.sy; } \\ (c) \text{ store } [y] \text{ 42 } \end{array} \parallel \begin{array}{l} (d) r_1 := \text{load } [y]; \text{ // 42 } \\ (e) r_2 := \text{load } [x + (r_1 - r_1)]; \text{ // 0 } \end{array}$$

$r_1 = 42 \wedge r_2 = 0$ forbidden

Our model accounts for this using *register views*:

- R8** The register state $\text{regs} : \text{Reg} \rightarrow (\text{Val} \times \mathbb{V})$ of a thread maps each register of the thread not only to a value, but

also to an associated view (of type \mathbb{V}). We write $v@v$ for a value-view pair.

- R9** When an instruction writes a register it also updates this view, to specify which writes have to have been seen in order to produce the value. For any arithmetic instruction, the view of the output register is the maximum of the views of its input registers; for a load it is the post-view (the maximum of its pre-view and read view).
- R10** Finally, the pre-view of a load or store is the maximal view of its input registers (for loads the registers in the “address expression”, for stores also that of the data) and the v_{rNew} or v_{wNew} view, respectively.

This will later be refined to handle more dependencies and *weaker barriers*, *release/acquire*, and *exclusives*.

Assuming the previous order a, b, c , when d reads $y = 42$, Thread 2 executes as follows:

$$\begin{array}{l} \langle \text{regs} = \{r_1 \mapsto 0@0, \dots\}, v_{rOld} = 0, v_{rNew} = 0 \rangle \\ \xRightarrow{(d)} \langle \text{regs} = \{r_1 \mapsto 42@2, \dots\}, v_{rOld} = 2, v_{rNew} = 0 \rangle \end{array}$$

Now, while $v_{rNew} = 0$, the pre-view of e is 2, because r_1 is one of its input registers. Therefore e is constrained by view 2, and thus cannot read the initial value $x = 0$.

Coherence Accessing the same location multiple times also induces constraints. Consider the following example, which adds a later, independent, load f to x to Thread 2. While f is not ordered with d , the execution where d reads $y = 42$, e reads $x = 37$ and f reads $x = 0$ is forbidden, since it violates the principle of *coherence*: a is ordered after the implicit initial $x = 0$ in memory. So if e has read $x = 37$, the program-order-later f must not read the coherence-superseded $x = 0$.

$$\begin{array}{l} (a) \text{ store } [x] \text{ 37; } \\ (b) \text{ dmb.sy; } \\ (c) \text{ store } [y] \text{ 42 } \end{array} \parallel \begin{array}{l} (d) r_1 := \text{load } [y]; \text{ // 42 } \\ (e) r_2 := \text{load } [x + (r_1 - r_1)]; \text{ // 37 } \\ (f) r_3 := \text{load } [x] \text{ // 0 } \end{array}$$

$r_1 = 42 \wedge r_2 = 37 \wedge r_3 = 0$ forbidden

To account for the architectural coherence requirements:

- R11** Each thread state maintains the coherence view $\text{coh} : \text{Loc} \rightarrow \mathbb{V}$. It maps a location x to the maximal post-view of all loads and stores on x executed so far by that thread.
- R12** A load or store on x is constrained not only by its pre-view, but also the coherence view $\text{coh}(x)$.

Since d reads $y = 42$ at timestamp 2, the register view of r_1 is 2, and so is the post-view of e . Thus, after e , the thread state is $\langle \text{coh} = \{x \mapsto 2, \dots\}, \dots \rangle$. Then, although the pre-view of f is 0, f is also constrained by $\text{coh}(x) = 2$, and thus cannot read the initial $x = 0$.

Store Forwarding However, while a load has to read from a write respecting coherence order, it does not have to effectively happen in order. Consider the next example, where Thread 1 is unchanged, but where Thread 2 now contains an earlier read d from y , followed by a write e of 51 to y , before the basic block of a read f from y followed by a read g from x with an address dependency on f . Assume d reads $y = 42$,

and f reads $y = 51$. While g is ordered after f by the address dependency, g is still allowed to read the initial $x = 0$: a load can “finish” before a same-thread store it reads from by *forwarding* when address and data of the store are determined, and so f can execute and resolve g 's dependency before e and even d .

$$\begin{array}{l} (a) \text{ store } [x] \text{ 37}; \\ (b) \text{ dmb.sy}; \\ (c) \text{ store } [y] \text{ 42} \end{array} \parallel \begin{array}{l} (d) r_0 := \text{load } [y]; \text{ // 42} \\ (e) \text{ store } [y] \text{ 51}; \\ (f) r_1 := \text{load } [y]; \text{ // 51} \\ (g) r_2 := \text{load } [x + (r_1 - r_1)] \text{ // 0} \end{array}$$

$r_0 = 42 \wedge r_1 = 51 \wedge r_2 = 0$ allowed

For d to read $y = 42$, our model must execute in the order a, b, c, d and then e , leading to memory $[1: \langle x := 37 \rangle_1; 2: \langle y := 42 \rangle_1; 3: \langle y := 51 \rangle_2]$. If f now were to read $y = 51$ at timestamp 3 its post-view would become 3, and so would the view of register r_1 ; this would not allow g to read the initial $x = 0$, since it would be constrained by pre-view 3 due to r_1 . To allow this behaviour, each thread state records information about the thread's own writes, and the definition of the read-view specially handles the case in which a load reads from a write by its own thread, to allow it to obtain a smaller post-view than the write's timestamp:

R13 Each thread state has a *forward bank* $\text{fwdb} : \text{Loc} \rightarrow \langle \text{time} : \mathbb{T}, \text{view} : \mathbb{V}, \text{xcl} : \mathbb{B} \rangle$ holding for each location x a record about the last write to x propagated by the thread:

R14 Whenever a thread executes a store to x it updates $\text{fwdb}(x)$ to record the timestamp of the write (time), the maximal view of the store's input registers (view), and whether it was a write exclusive (xcl). I.e. view captures its address and data dependencies.

R15 Initially, $\text{fwdb}(x)$ is $\langle \text{time} = 0, \text{view} = 0, \text{xcl} = \text{false} \rangle$ for any location x .

R16 The read-view of a load to some location x is refined as follows: if the read message's timestamp equals $\text{fwdb}(x).\text{time}$ (i.e. the load reads the last write at x by its thread), its read-view is the associated forward view $\text{fwdb}(x).\text{view}$. Otherwise it is the read message's timestamp, as before.

Since the post-view of a load includes the read-view, the latter means that when reading by forwarding the post-view contains the address and data dependencies of the write instead of the write's timestamp. The xcl is only for exclusive instructions (§A.2).

In the example above, d reads $y = 42$ at timestamp 2, updating $\text{coh}(y)$ to 2; e writes $y = 51$ at timestamp 3, updating $\text{coh}(y)$ to 3 and $\text{fwdb}(y)$ to $\langle \text{time} = 3, \text{view} = 0, \text{xcl} = \text{false} \rangle$, since e has no input register; f reads $y = 51$ at timestamp 3, with pre-view 0, read-view 0 and post-view 0, since the forward view of the write $y = 51$ is $\text{fwdb}(y).\text{view} = 0$, thereby setting the view of r_1 to 0; finally, g can read the initial $x = 0$ with pre-view 0, since its sole input register, r_1 , has view 0.

It is important to note that, as seen in this example, in general the coherence view $\text{coh}(x)$ on a location x is never

merged into any other views such as pre-views, post-views and register-views, so that its effect is limited to loads and stores on location x only.

4.2 Promising Semantics

In ARMv8/RISC-V, stores can be executed out of order, too. PROMISING-ARM/RISC-V models such behaviours by adding the notion of *promises* on top of the view semantics presented so far. As a motivating example, consider the next program. Here Thread 1 reads from x , and writes the value it reads to y ; Thread 2 reads from y , and writes 42 to x . So far, we have not introduced any mechanism that would allow both a and c to read values different from 0: at least one of a and c would have to have executed first in the initial memory, and therefore would have to read 0.

$$\begin{array}{l} (a) r_1 := \text{load } [x]; \text{ // 42} \\ (b) \text{ store } [y] r_1 \end{array} \parallel \begin{array}{l} (c) r_2 := \text{load } [y]; \text{ // 42} \\ (d) \text{ store } [x] \text{ 42} \end{array}$$

$r_1 = r_2 = 42$ allowed

However, since d is independent of c , in ARMv8/RISC-V it is allowed to execute early, and so both a and c can read 42, which corresponds to an execution order d, a, b, c .

Promises To model out-of-order execution of writes, we add the notions of promise and fulfilment.

R17 Each thread state maintains a set of timestamps $\text{prom} : \text{set } \mathbb{T}$, called its *promise set*, which records the timestamps of the outstanding promised writes of the thread.

R18 A thread with ID tid is allowed to *promise* a write $x = v$, which appends $\langle x := v \rangle_{\text{tid}}$ to memory and adds the timestamp t of the write message $\langle x := v \rangle_{\text{tid}}$ to prom , but does not otherwise change the thread state. As far as other threads are concerned, this write is no different from other writes in memory (prom is thread-local information).

R19 The thread is required to *fulfil* this promise $x = v$ at timestamp t at a later stage by executing a store instruction, removing the promise from prom . Specifically, the store must generate a write $x = v$ whose pre-view and coherence view $\text{coh}(x)$ are strictly smaller than the promise timestamp t .

R20 We split the execution of a write into a promise and its fulfilment. A normal write that is not executed early is accounted for by promising it just before a store fulfils it.

(We explain later exactly how executions with unfulfilled promises are prevented and how the executable model computes the possible promises in a given state.)

Note that the timestamp of a write is always bigger than its pre-view because it is appended at the end of memory with a fresh timestamp and immediately fulfilled.

The pre-view of a store essentially constrains promises by constraining the fulfilment: a promise cannot be made “too early”, because it cannot be fulfilled if its timestamp is not strictly larger than its pre-view. With only these rules added

to the underlying view semantics, in what follows, we show how promises capture the out-of-order execution of stores.

Out-of-order Execution of Writes The behaviour in the previous example is explained as follows. Thread 2 first promises write $x = 42$ at timestamp 1, resulting in promise set $\text{prom} = \{1\}$ and memory $[1: \langle x := 42 \rangle_2]$. Now, on Thread 1 a can read $x = 42$ and write $y = 42$ (by a normal write), resulting in memory $[1: \langle x := 42 \rangle_2, 2: \langle y := 42 \rangle_1]$. Then, c can read $y = 42$, and d can fulfil the promise $x = 42$ at timestamp 1, yielding $\text{prom} = \{\}$; d 's pre-view and $\text{coh}(x)$ are 0, strictly smaller than the promise timestamp 1, as required.

Memory Barriers Placing a barrier on Thread 2 prevents the out-of-order execution of writes.

$$\begin{array}{l} (a) r_1 := \text{load } [x]; // 42 \\ (b) \text{store } [y] r_1 \end{array} \parallel \begin{array}{l} (c) r_2 := \text{load } [y]; // 42 \\ (d) \text{dmb.sy}; \\ (e) \text{store } [x] 42 \end{array} \\ r_1 = r_2 = 42 \text{ forbidden}$$

The model handles this using views. As before, consider the state after Thread 2 promised $x = 42$ and Thread 1 executed a, b , resulting in memory $[1: \langle x := 42 \rangle_2, 2: \langle y := 42 \rangle_1]$. Here, c is not allowed to read $y = 42$, because Thread 2 would not be able to fulfil the promise at timestamp 1. Suppose c does read $y = 42$ at timestamp 2. Then Thread 2 has $v_{\text{Old}} = 2$ after c and $v_{\text{New}} = 2$ by dmb.sy after d . Then the pre-view of e is 2 due to v_{New} , which is not smaller than the promise timestamp 1. If, instead, c reads the initial $y = 0$, e can fulfil the promise.

Coherence Also, replacing d by $r_3 := \text{load } [x + (r_2 - r_2)]$ constrains e by coherence and forbids the same behaviour. To illustrate, suppose we execute up to c as before. Since c reads $y = 42$ and thus r_2 holds $42@2$, d is constrained by pre-view 2 and must read $x = 42$ at timestamp 1. Now although r_2 and r_3 are not used by e , e still cannot fulfil its promise of $x = 42$ at timestamp 1 since d updated $\text{coh}(x)$ to its post-view 2 and e is constrained by $\text{coh}(x) = 2 \not\prec 1$.

Address and Data Dependencies Replacing the barrier on Thread 2 by a dependency from the load to the store — whereby the address or data of the store depends on the result of the load — also prevents the behaviour. Similarly to before, consider the execution in which Thread 2 promises $x = 42$ at timestamp 1, a reads $x = 42$, b writes $y = 42$ at timestamp 2, and c reads $y = 42$, thereby setting r_2 's register view to 2. Here d 's pre-view includes r_2 's register view 2, and so d cannot fulfil the promise at timestamp 1. Changing d to 'store $[x] (42 + (r_2 - r_2))$ ' leads to the same behaviour.

$$\begin{array}{l} (a) r_1 := \text{load } [x]; // 42 \\ (b) \text{store } [y] r_1; \end{array} \parallel \begin{array}{l} (c) r_2 := \text{load } [y]; // 42 \\ (d) \text{store } [x + (r_2 - r_2)] 42 \end{array} \\ r_1 = r_2 = 42 \text{ forbidden}$$

Control and Address-po Dependencies While in ARMv8 and RISC-V loads are allowed to execute speculatively past conditional branches, stores are not. Control dependencies order writes with respect to reads affecting the control flow. Similarly, stores wait for the address of all program-order-earlier memory accesses to be determined (*address-po* dependency). Placing a conditional branch depending on c 's return value before the write of x also prevents promising it early: the behaviour in which both a and c read 42 is forbidden in the example below, due to the control dependency of e on c .

$$\begin{array}{l} (a) r_1 := \text{load } [x]; // 42 \\ (b) \text{store } [y] r_1 \end{array} \parallel \begin{array}{l} (c) r_2 := \text{load } [y]; // 42 \\ (d) \text{if } ((r_2 - r_2) = 0) \\ (e) \text{store } [x] 42 \end{array} \\ r_1 = r_2 = 42 \text{ forbidden}$$

To capture such dependencies we introduce the view v_{CAP} .

- R21** Each thread state has a view $v_{\text{CAP}} : \mathbb{V}$, initially set 0.
- R22** Whenever a thread executes a conditional branch, the maximal view of the branch's input registers is merged into v_{CAP} . Similarly, when a load or store is executed, the maximal view of the input registers used to compute the address is merged into v_{CAP} .
- R23** Finally, the pre-view of a store instruction is refined to include v_{CAP} (*i.e.* the pre-view is the maximal view of the input registers and v_{wNew} and v_{CAP}).

Assume again an execution in which $x = 42$ is promised at timestamp 1 by Thread 2, a reads $x = 42$, b writes $y = 42$ at timestamp 2, and c reads $y = 42$, thereby setting r_2 's view to 2. Then d merges r_2 's view (2) into v_{CAP} since r_2 is used to compute the branch condition. In case d is store $[z + (r_2 - r_2)] 0$, register r_2 's view is also merged into v_{CAP} since r_2 is used to compute the address. Then e 's pre-view includes $v_{\text{CAP}} = 2$, and thus e cannot fulfil the promise at timestamp 1. Replacing d by an address-dependent load or store to an otherwise unused memory location z (e.g. store $[z + (r_2 - r_2)] 0$) introduces the same ordering and also forbids the behaviour.

Release/Acquire, Weaker Barriers, Load/Store Exclusives In addition to the full dmb.sy barriers ARMv8 and RISC-V also have a number of weaker barriers; both also have release/acquire instructions, so-called half-barriers. Moreover, ARMv8 and RISC-V have load/store exclusive instructions (called load reserve and store conditional in RISC-V) that provide inter-thread *atomicity guarantees*: when a load exclusive r pairs with a program-order-later store exclusive w from the same thread and to the same location, the architectures guarantee exclusive access to this location to the thread if the store exclusive succeeds; otherwise the store fails.

For space reasons we omit the details on these instructions in §5. The instructions are natural extensions to the model and the supplementary material (§A) contains the full model

definition including these; the Coq formalisation and proof, and the executable model both handle these instructions.

4.3 Certification

Our description so far has focussed on the thread steps and has assumed *consistent traces*, traces in which all promises are fulfilled. Indeed, the semantics given by traces of these thread steps, restricted to consistent traces, precisely models the legal behaviours of ARMv8/RISC-V (*i.e.*, is equivalent to the axiomatic model): (combining Theorems 6.1 and 6.2).

However, we have not yet discussed how the model ensures threads only take consistent steps (steps of consistent executions). Rather than merely discarding traces with unfulfilled promises at the end of the execution, directly preventing inconsistent thread steps is desirable for two reasons: (1) The model works incrementally in terms of thread-local conditions, thereby also improving interactive exploration. (2) It removes unnecessary non-determinism resulting from promises that eventually are unfulfilled, for executability and exhaustive exploration.

We now show how such inconsistent thread steps can be prevented. To this end, we first define what it means for a thread to *execute sequentially*. It means that the thread executes alone (no other threads executing) and every new promise is immediately followed by its fulfilment (effectively doing all writes in program-order). The model then prevents inconsistent thread steps using a simple, thread-local definition of *certification*, allowing any given thread step only if it leads to a *certified thread configuration*.

R24 A thread configuration $\langle T, M \rangle$, consisting of a thread state T and memory state M is *certified* if there exists a sequential execution from $\langle T, M \rangle$ to another thread configuration $\langle T', M' \rangle$ such that T' has no outstanding promises.

Restricting thread steps to steps certified as above, is *sound*, not preventing any consistent executions (See Theorem 6.2). For RISC-V, this definition is also *precise*, preventing any inconsistent executions (Theorem 6.3).

In ARMv8, however, it is not precise. Whereas generally, syntactic dependencies create memory ordering, in ARMv8, dependencies from a store exclusive's status register write are an exception. The consequence in our model is the following: if a thread t makes a promise that relies on some store exclusive s succeeding, it can do this even before s is propagated. If s later turns out to conflict with the write of another thread and fails, t cannot fulfil its promises. The certification definition above does not prevent this, for the same reasons that Flat suffers from such deadlocks [39]. The supplementary material (§C.2) details these issues and discusses a prototype extension of the model with locks and a more sophisticated certification that takes locking into account to prevent deadlocks.

The above definition provides a simple executable check for whether a thread configuration is certified. However,

the executable tool of §7 has to be able to compute for any given thread state *which* promises should be allowed: which promises lead to such certified configurations.

For the sake of the executable model, we give an equivalent algorithmic definition, called `find_and_certify`, that we proved correct in Coq (Theorem 6.4). To enumerate which promises a thread tid in configuration $\langle T, M \rangle$ is allowed to do, the algorithm works as follows:

1. Enumerate all possible traces of tid executing *sequentially*: this thread executing alone under current memory. (For programs with infinite loops the user can bound the depth.)
2. Discard the traces in which the final state of tid has unfulfilled promises.
3. For any remaining trace t : any write done during t is a legal promise step if its store's *pre-view* and *coherence-view* (at its location) are less than or equal to the maximal timestamp of the current memory M (the memory before the start of the certification).

Section B of the supplementary material gives an example for this algorithm.

5 The Model, Formally

Fig. 2 defines the types, Fig. 3 the rules of the model. For simplicity, values and addresses are mathematical integers. Note that some of the types are not used by the rules shown here, but used by the full definition of §A of the supplementary material that handles weaker barriers, release/acquire, and load/store exclusive instructions. For the common instructions, ARM and RISC-V only differ in acquire and exclusive instructions. The description cross-references the §4 rules.

Auxiliaries The expressions interpretation function (second and third line) takes an expression and a register state m , and returns the expression's value and view. Constants have view 0; registers are looked up in m ; the view for an arithmetic expression merges the arguments' views (**R9**). `read(M, l, t)` gives the result of reading location l at timestamp t in memory M : for $t = 0$ the initial value v_{init} , here 0; otherwise either the value of the message in M at timestamp t if its location is l or *none*. `read-view(a, rk, f, t)` returns either the timestamp t of the read message or the forward view of the message f in the forward bank (**R13** – **R16**). Now we define thread-local steps, which do not change memory.

Thread-local Steps $T, M \xrightarrow[tid]{l} T'$

FULFIL. This transition is annotated with the timestamp t of the promise that is being fulfilled. (Other thread-local steps do not have the timestamp annotation.) The definition starts with the pre-condition (from top to bottom). First evaluate address and data expressions. Since we assume writes always promise first and then fulfil, this step requires the write to have been promised. Rules **R10**, **R6**, **R21** describe the components contributing to the pre-view. The pre-view

$$\begin{array}{l}
l \in \text{Loc} \stackrel{\text{def}}{=} \text{Val} \quad v \in \text{Val} \stackrel{\text{def}}{=} \mathbb{Z} \quad \text{tid} \in \text{Tid} \stackrel{\text{def}}{=} \mathbb{N} \quad t \in \mathbb{T} \stackrel{\text{def}}{=} \mathbb{N} \quad v \in \mathbb{V} \stackrel{\text{def}}{=} \mathbb{T} \\
w \in \text{Msg} \stackrel{\text{def}}{=} \langle \text{loc} : \text{Loc}; \text{val} : \text{Val}; \text{tid} : \text{Tid} \rangle \quad \langle x := v \rangle_{\text{tid}} \stackrel{\text{def}}{=} \langle \text{loc} = x; \text{val} = v; \text{tid} = \text{tid} \rangle \quad M \in \text{Memory} \stackrel{\text{def}}{=} \text{list Msg} \\
ts \in \text{TState} \stackrel{\text{def}}{=} \left\langle \begin{array}{l} \text{prom} : \text{set } \mathbb{T}; \quad \text{regs} : \text{Reg} \rightarrow \text{Val} \times \mathbb{V}; \\ \text{coh} : \text{Loc} \rightarrow \mathbb{V}; \quad v_{\text{rOld}}, v_{\text{wOld}}, v_{\text{rNew}}, v_{\text{wNew}}, v_{\text{CAP}}, v_{\text{Rel}} : \mathbb{V}; \\ \text{fwdb} : \text{Loc} \rightarrow \langle \text{time} : \mathbb{T}; \text{view} : \mathbb{V}; \text{xcl} : \mathbb{B} \rangle; \\ \text{xclb} : \text{option } \langle \text{time} : \mathbb{T}; \text{view} : \mathbb{V} \rangle \end{array} \right\rangle \quad \begin{array}{l} T \in \text{Thread} \stackrel{\text{def}}{=} \text{St} \times \text{TState} \\ \vec{T} \in \text{TPool} \stackrel{\text{def}}{=} \text{Tid} \rightarrow \text{Thread} \\ \langle \vec{T}, M \rangle \in \text{Machine} \stackrel{\text{def}}{=} \text{TPool} \times \text{Memory} \end{array}
\end{array}$$

Figure 2. Types in the semantics

$$\begin{array}{l}
c ? v_1 : v_2 \stackrel{\text{def}}{=} \text{if } c \text{ then } v_1 \text{ else } v_2 \quad c ? v \stackrel{\text{def}}{=} c ? v : 0 \quad v_1 \sqcup v_2 \stackrel{\text{def}}{=} \max(v_1, v_2) \quad v @ v \stackrel{\text{def}}{=} \langle v, v \rangle : \text{Val} \times \mathbb{V} \\
\llbracket (-) \rrbracket_{(-)_2} : \text{Expr} \rightarrow (\text{Reg} \rightarrow \text{Val} \times \mathbb{V}) \rightarrow \text{Val} \times \mathbb{V} \\
\llbracket v \rrbracket_m \stackrel{\text{def}}{=} v @ 0 \quad \llbracket r \rrbracket_m \stackrel{\text{def}}{=} m(r) \quad \llbracket e_1 \text{ op } e_2 \rrbracket_m \stackrel{\text{def}}{=} (v_1 \llbracket \text{op} \rrbracket v_2) @ (v_1 \sqcup v_2) \text{ with } \llbracket e_1 \rrbracket_m = v_1 @ v_1, \llbracket e_2 \rrbracket_m = v_2 @ v_2
\end{array}$$

$$\text{read}(M, l, t) : \text{option Val} \stackrel{\text{def}}{=} \text{if } t = 0 \text{ then } v_{\text{init}} \text{ else (if } M(t).\text{loc} = l \text{ then } M(t).\text{val} \text{ else none)}$$

$$\text{read-view}(a, rk, f, t) \stackrel{\text{def}}{=} (f.\text{time} = t) ? f.\text{view} : t$$

<div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">$T, M \xrightarrow{t}_{\text{tid}} T'$</div> <p>(READ)</p> $ \begin{array}{l} l @ v_{\text{addr}} = \llbracket e \rrbracket_{ts.\text{regs}} \quad \text{read}(M, l, t) = v \quad v_{\text{pre}} = v_{\text{addr}} \sqcup ts.v_{\text{rNew}} \\ \forall t'. t < t' \leq (v_{\text{pre}} \sqcup ts.\text{coh}(l)) \implies M(t').\text{loc} \neq l \\ v_{\text{post}} = v_{\text{pre}} \sqcup \text{read-view}(a, rk, ts.\text{fwdb}(l), t) \\ ts' = ts \left[\begin{array}{l} \text{regs}(r) \mapsto v @ v_{\text{post}}, \quad \text{coh}(l) \mapsto ts.\text{coh}(l) \sqcup v_{\text{post}}, \\ v_{\text{rOld}} \mapsto ts.v_{\text{rOld}} \sqcup v_{\text{post}}, \quad v_{\text{CAP}} \mapsto ts.v_{\text{CAP}} \sqcup v_{\text{addr}} \end{array} \right] \\ \hline \langle r := \text{load}_{\text{false}, rk} [e], ts \rangle, M \rightarrow_{\text{tid}} \langle \text{skip}, ts' \rangle \end{array} $	<p>(FULFIL)</p> $ \begin{array}{l} \llbracket e_1 \rrbracket_{ts.\text{regs}} = l @ v_{\text{addr}} \quad \llbracket e_2 \rrbracket_{ts.\text{regs}} = v @ v_{\text{data}} \quad t \in ts.\text{prom} \\ M(t) = \langle l := v \rangle_{\text{tid}} \quad v_{\text{pre}} = v_{\text{addr}} \sqcup v_{\text{data}} \sqcup ts.v_{\text{wNew}} \sqcup ts.v_{\text{CAP}} \\ v_{\text{pre}} \sqcup ts.\text{coh}(l) < t \quad v_{\text{post}} = t \\ ts' = ts \left[\begin{array}{l} \text{prom} \mapsto ts.\text{prom} \setminus \{t\}, \quad \text{coh}(l) \mapsto ts.\text{coh}(l) \sqcup v_{\text{post}}, \\ v_{\text{wOld}} \mapsto ts.v_{\text{wOld}} \sqcup v_{\text{post}}, \quad v_{\text{CAP}} \mapsto ts.v_{\text{CAP}} \sqcup v_{\text{addr}}, \\ \text{fwdb}(l) \mapsto \langle \text{time} = t; \text{view} = v_{\text{addr}} \sqcup v_{\text{data}}; \text{xcl} = \text{false} \rangle \end{array} \right] \\ \hline \langle r_{\text{succ}} := \text{store}_{\text{false}, wk} [e_1] e_2, ts \rangle, M \xrightarrow{t}_{\text{tid}} \langle \text{skip}, ts' \rangle \end{array} $		
<p>(DMB)</p> $ \begin{array}{l} v = ts.v_{\text{rOld}} \sqcup ts.v_{\text{wOld}} \\ ts' = ts \left[\begin{array}{l} v_{\text{rNew}} \mapsto ts.v_{\text{rNew}} \sqcup v, \\ v_{\text{wNew}} \mapsto ts.v_{\text{wNew}} \sqcup v \end{array} \right] \\ \hline \langle \text{fence}_{K_1, K_2}, ts \rangle, M \rightarrow_{\text{tid}} \langle \text{skip}, ts' \rangle \end{array} $	<p>(REGISTER)</p> $ \begin{array}{l} ts' = ts[\text{regs}(r) \mapsto \llbracket e \rrbracket_{ts.\text{regs}}] \\ \hline \langle r := e, ts \rangle, M \rightarrow_{\text{tid}} \langle \text{skip}, ts' \rangle \end{array} $	<p>(BRANCH)</p> $ \begin{array}{l} \llbracket e \rrbracket_{ts.\text{regs}} = v @ v \\ ts' = ts[v_{\text{CAP}} \mapsto ts.v_{\text{CAP}} \sqcup v] \\ \hline \langle \text{if } (e) s_1 s_2, ts \rangle, M \rightarrow_{\text{tid}} \langle v \neq 0 ? s_1 : s_2, ts' \rangle \end{array} $	
<p>(SKIP)</p> $ \begin{array}{l} \langle \text{skip}; s, ts \rangle, M \rightarrow_{\text{tid}} \langle s, ts \rangle \end{array} $	<p>(SEQ)</p> $ \begin{array}{l} \langle s_1, ts \rangle, M \rightarrow_{\text{tid}} \langle s'_1, ts' \rangle \\ \hline \langle s_1; s_2, ts \rangle, M \rightarrow_{\text{tid}} \langle s'_1; s_2, ts' \rangle \end{array} $	<p>(WHILE)</p> $ \begin{array}{l} s' = \text{if } (e) (s; \text{while } (e) s) \text{ skip} \\ \hline \langle \text{while } (e) s, ts \rangle, M \rightarrow_{\text{tid}} \langle s', ts \rangle \end{array} $	<div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">$\langle T, M \rangle \xrightarrow{\text{seq}}_{\text{tid}} \langle T', M' \rangle$</div> <p>(SEQ-EXEC)</p> $ \begin{array}{l} T, M \rightarrow_{\text{tid}} T' \\ \hline \langle T, M \rangle \xrightarrow{\text{seq}}_{\text{tid}} \langle T', M' \rangle \end{array} $ <p>(SEQ-WRITE)</p> $ \begin{array}{l} \langle T, M \rangle \xrightarrow{t}_{\text{tid}} \langle T', M' \rangle \\ T', M' \xrightarrow{t}_{\text{tid}} T'' \\ \hline \langle T, M \rangle \xrightarrow{\text{seq}}_{\text{tid}} \langle T'', M' \rangle \end{array} $
<div style="border: 1px solid black; padding: 2px; margin-bottom: 5px;">$\langle T, M \rangle \xrightarrow{t}_{\text{tid}} \langle T', M' \rangle$</div> <p>(EXECUTE)</p> $ \begin{array}{l} T, M \rightarrow_{\text{tid}} T' \\ \hline \langle T, M \rangle \rightarrow_{\text{tid}} \langle T', M' \rangle \end{array} $	<p>(PROMISE)</p> $ \begin{array}{l} w.\text{tid} = \text{tid} \quad t = M + 1 \quad ts' = ts[\text{prom} \mapsto ts.\text{prom} \cup \{t\}] \\ \hline \langle \langle s, ts \rangle, M \rangle \xrightarrow{t}_{\text{tid}} \langle \langle s, ts' \rangle, M + [w] \rangle \end{array} $	<p>(MACHINE-STEP)</p> $ \begin{array}{l} \langle \vec{T}[\text{tid}], M \rangle \rightarrow_{\text{tid}} \langle T', M' \rangle \quad \langle T', M' \rangle \text{ certified} \\ \hline \langle \vec{T}, M \rangle \rightarrow \langle \vec{T}[\text{tid} \mapsto T'], M' \rangle \end{array} $	<p>$\langle T, M \rangle \text{ certified} \stackrel{\text{def}}{=} \exists T', M'. \langle T, M \rangle \xrightarrow{\text{seq}}_{\text{tid}}^* \langle T', M' \rangle \wedge T'.\text{prom} = \{ \}$</p>

Figure 3. Formal definition of the model, including Thread-local steps, thread steps, and machine steps

and coherence view have to be less than t (**R19**); the post-view is the timestamp t (**R3**). The post-condition removes the promise (**R19**) and updates the coherence view to include t (**R11**), certain views (**R5**, **R22**); the forward bank (**R14**). **O READ** also starts with the pre-condition (from top to bottom). First evaluate the address l ; in order to read v it must be $v = \text{read}(M, l, t)$ as described above. The pre-view calculation is described in **R10**, **R6**. The pre-view (**R2**) and the

coherence view (**R12**) constrain the read. The post-view is defined in **R3**, **R16**. The post-condition updates the register with value and post-view (**R9**); coherence with post-view as in rule **R11**; and views as in **R5**, **R22**.

DMB is the rule for strong barriers (`dmb.sy` in ARMv8 and `fenceRW, RW` in RISC-V). It updates v_{rNew} and v_{wNew} , to include v_{rOld} and v_{wOld} according to the intuition given in **R5**,

R6. The definition matches rules **R5** – **R7**. **REGISTER** A register assignment updates the register with the expressions and view from the evaluation of its expression (**R9**). **BRANCH:** The pre-condition evaluates the condition, branches as determined by this value, and updates v_{CAP} (**R22**). **SKIP, SEQ, and WHILE:** mostly as expected.

Thread Steps $\langle T, M \rangle \xrightarrow{[t]}_{tid} \langle T', M' \rangle$

EXECUTE lifts a thread-local step that does not change memory to a thread step. **PROMISE** allows promising any write message, appending this write to memory and recording its timestamp in prom. As thread-local steps, thread steps can be annotated with a timestamp t ; this is used for the steps for promising and for promise fulfilment. While thread steps allow unconstrained promises, machine steps only allow certified promises. Note that “normal writes” are modelled as promises immediately followed by fulfilment.

Machine Steps $\langle \vec{T}, M \rangle \rightarrow \langle \vec{T}', M' \rangle$

Lifts *certified* thread steps (**R24**).

6 Proof

In Coq, we formally prove equivalence to the ARMv8 and RISC-V axiomatic models, deadlock freedom for RISC-V, and correctness of `find_and_certify`. The former currently assumes known simplifications of the axiomatic models, to unify ARMv8 and RISC-V for the Coq proof. We call the unified model **AXIOMATIC** (see supplementary material §D).

Theorem 6.1. *For a program p , \vec{R} is a final register state of a legal candidate execution of p in **AXIOMATIC** if and only if it is that of a valid execution of p in **PROMISING-ARM/RISC-V**.*

Theorem 6.2. *Moreover, **PROMISING-ARM/RISC-V** is equivalent to **PROMISING-ARM/RISC-V** without certification.*

Theorem 6.3 (Deadlock freedom). *For any machine state in **PROMISING-RISC-V** where every thread state of it is certified, there exists an execution to a machine state with no promises.*

Theorem 6.4 (Correctness of `find_and_certify`). *Assume the thread configuration $\langle T, M \rangle$ is certified, and promising p leads to $\langle T', M' \rangle$. Then $\langle T', M' \rangle$ is certified if and only if $p \in \text{find_and_certify}(T, M)$.*

7 Executable Tool

Exhaustively enumerating all outcomes of a concurrent program is combinatorially challenging. The main optimisation the executable tool incorporates is based on the following key property of the model, proved in Coq.

Theorem 7.1. *For every **PROMISING** trace tr , there exists a trace tr' with same final state such that tr' can be split into a sequence of promise transitions followed by only non-promise transitions.*

The model uses this property as follows: (1) The model starts in “promise-mode”, exploring all possible interleavings of only promise transitions. (2) Once reaching a state in which it is possible to continue executing with no further promises it can enter “non-promise-mode”. Here no promise transitions are enabled. Since the memory is now fixed, the remaining execution of the threads is completely independent. Hence, the model can compute all outcomes of a given program by first enumerating all “final memories”, interleaving only promise transitions, and then exploring which final thread states are possible under this memory without interleaving any reads, greatly reducing the non-determinism.

Another optimisation we implement allows the user to supply information about which memory locations are shared between threads and which are purely thread-local. The model then treats accesses to non-shared locations as register reads/writes, again reducing the interleavings. In order to prevent user errors, the model could check that non-shared locations are accessed by one thread only. (The model currently does not, but it is an easy addition.) Moreover, we plan to extend the model to automatically derive this information, using existing mechanisms for promise certification.

Executable Model The executable model closely follows the Coq definitions where possible, but differs from it in two ways. Firstly, the executable model does not use OCaml code automatically produced by Coq, since interfacing with the existing rmem and Sail infrastructure would be difficult. Secondly, while the Coq model formalises the small imperative language, the executable model integrates definitions for user-mode ARMv8 and RISC-V instructions, meaning it needs logic for computing the views of loads and stores of the ISA definitions [13, 22]. (Like Flat, our Sail model does not yet include ARM’s weaker load acquire LDAPR introduced in ARMv8.3. We do cover its concurrency behaviour in the Coq model.) We ensured our model also experimentally agrees with the axiomatic models on suites of around 6,500 litmus tests for ARMv8 and 7,000 for RISC-V (150 RISC-V tests we cannot run because they have AMO instructions).

8 Tool Use and Evaluation

To evaluate the exploration tool, we test several standard datastructure and lock implementations, for ARMv8. We first demonstrate the use of the tool for one of the examples and then give a summary of all results and run times. The code of all examples is in the supplementary material.

Example Use Case We consider the Michael & Scott queue, a queue allowing concurrent enqueueing and dequeueing [36] that we implement in C++. To the code for the actual data structure we add test code: three threads running in parallel, each doing enqueue and dequeue operations while recording which data they enqueue and dequeue. The source

altogether has 215 lines of C++ code, which we compile using a standard GCC 6.3.0 cross compiler with `-O3`, obtaining 472 lines of assembly code. We then run a script that maps the assembly into the *litmus* format used by *herd* and *rmem*: our tool does not support dynamic thread creation yet; the *litmus* format allows writing the code directly as a parallel thread composition. Another limitation is that our tool does not yet support dynamic memory allocation, which we “fake” here with a very naive `malloc` as part of the source code (see code). We are planning to add dynamic thread creation and memory allocation, which just requires additional engineering.

Running our model exhaustively, integrated into *rmem*, outputs the list of possible final outcomes and allows us to check whether the code has behaved correctly. For a version in which Thread 1 enqueues once and Threads 2 and 3 each try to dequeue once the tool finishes in 9 seconds, reporting no incorrect state. We also try other versions (see Table 2), finding no incorrect states.

When implementing the queue, we initially chose conservative acquire/release ordering for all but two C++ atomic accesses. Investigating the assembly shows the assembly code under ARM’s memory model provides stronger guarantees than required. We experiment with relaxing some of the atomics and run the tool again. After roughly two minutes it reports an incorrect state: one in which the enqueue operation succeeded, the queue is empty, but neither of the dequeuing threads has read the data. The tool also provides a witnessing trace, that allows interactively stepping through the execution for debugging. (Table 2 shows numbers for an optional optimisation, but for which the model currently does not produce fine-grained interactive traces; this just requires additional engineering.)

In this case, we see the following behaviour. The first transitions are all promising transitions by the enqueueing thread, Thread 1, partly for initialising the queue. The queue is implemented as a linked list. Each queue element is a struct with two fields, `data` and `next`, a pointer to the next element. The queue contains an initial dummy element, `Init`, and fields `head` and `tail` pointing to start and end of the queue. Thread 1 sets these up: it writes `Init` with `data = 0` and `next = null`, and points `head` and `tail` to `Init`. Thread 1 also does the first enqueue operation, of an element `e`. The steps are, in program order:

1. create the new element `e`, with `next = null` and `data` (in this case) set to 1,
2. and enqueue `e`: find the tail of the queue, here `Init`, and set its `next` field to point to `e`.

In this trace, the problematic behaviour occurs in the third transition: Thread 1 writes `Init`’s `next` field to point to `e`, before having written `e`’s data (executing step 2 before step 1). Thus, later, when Thread 2 dequeues `e`, it can read the initial value 0 for `e`’s data, even though 1 would be correct.

Here the bug is easily fixed, by making the above two steps execute in program-order. We fix the issue by making the

Table 1. *LOC* = assembly lines, *Ts* = number of threads

<i>Test</i>	<i>Lang</i>	<i>LOC</i>	<i>Ts</i>	<i>Test</i>	<i>Lang</i>	<i>LOC</i>	<i>Ts</i>
SLA	ARMv8	44	2	TL	C++	120	3
SLC	C++	51	3	STC	C++	366	3
SLR	Rust	84	3	STR	Rust	393	3
PCS	C++	69	2	DQ	C++	247	3
PCM	C++	130	3	QU	C++	473	3

write of the next field in step 2 a release write, preventing “publishing” the new element before its data has been written. The resulting code is unsound in C++ but still sound in ARM.

Tested Examples and Results We give an overview of the tests we ran in Table 1. We test, from simple to complex: three different spinlock variants, implemented in assembly (SLA), C++ (SLC), and Rust (SLR), where Linux-Spinlock (SLA) is an example taken from a Linux kernel spinlock implementation [25, 33], which was also used by Pulte et al. [39] for demonstrating Flat² (their other test, `spin_unlock_wait`, requires mixed-size support); single-producer-single-consumer (PCS) and single-producer-multiple-consumers (PCM) circular queues; a ticket lock (TL); Treiber stack [17], separately implemented in C++ (STC) and Rust (STR); Chase-Lev dequeue (DQ) [28, 32]; and the aforementioned variants of the Michael & Scott queue (QU). In addition, for the last four examples we also try versions optimised for ARMv8. Table 2 shows selected results, more in the supplementary material (SE). All programs in C++ and Rust are compiled with GCC 6.3.0 and RUSTC 1.30 with optimization level 3. All numbers are from a standard desktop machine, Ubuntu 16.04 Intel Core i7-7700 at 3.60GHz, 8GB memory.

The names mean the following. For the spinlock tests: `spinlock-n` means `n` loop unrollings on all threads; `PCM-n-n-n`: Thread 1 producing `n` times, Threads 2 and 3 consuming `n` times; `PCS-n-n` the same for Thread 1 producing, Thread 2 consuming; `TL-n`: threads spin `n` times to acquire lock; `STC/R-abc-def-ghi`: Thread 1 pushing `a` times, popping `b` times, and again pushing `c` times, and analogously for Thread 2 with `def` and Thread 3 with `ghi`; `DQ/(opt)-abc-d-e`: Thread 1 pushes `a` times, pops `b` times, and pushes `c` times, Thread 2 steals `d` times, and Thread 3 steals `e` times; `QU/(opt)-abc-def-ghi`: Thread 1 enqueues `a` times, dequeues `b` times, and enqueues `c` times again, analogously with `def` for Thread 2 and `ghi` for Thread 3.

We tried running the examples on *herd*, but all but the spin and ticket locks (SLC,SLR,TL) require instructions unsupported by *herd*. For SLC and TL, we ran the tests on *herd*:

- SLC-1: 14.72 sec, (Promising: 3.21 sec)
- SLC-2: stack overflow in 123.51 sec, (Promising: 4.69 sec)
- TL-1: 31.04 sec, (Promising: 10.16 sec)

²We change mixed-size loads in the example to same-size and confirmed that performance is unaffected.

Table 2. Run times in seconds. ooT = more than four hours.

<i>Test</i>	<i>Promising</i>	<i>Flat</i>
SLA-7	0.61	9108.53
SLC-3	6.58	1472.74
SLR-3	4.88	52.52
PCS-3-3	1.36	249.26
PCM-3-3-3	71.12	ooT
TL/(opt)-3	18.08 / 20.13	ooT / ooT
STC/(opt)-100-010-010	0.42 / 0.42	2144.52 / 5943.50
STC/(opt)-100-100-010	8.70 / 8.70	ooT / ooT
STC/(opt)-210-011-000	615.41 / 637.98	ooT / ooT
STR-100-010-010	0.39	77.21
STR-100-100-010	7.30	8940.03
STR-210-011-000	522.19	ooT
DQ/(opt)-100-1-0	0.30 / 0.30	2.93 / 2.97
DQ/(opt)-110-1-0	0.44 / 0.44	1042.88 / 1114.39
DQ/(opt)-211-2-1	28.55 / 111.54	ooT / ooT
QU/(opt)-100-000-000	1.34 / 2.95	2983.11 / ooT
QU/(opt)-100-010-000	2.55 / 5.66	ooT / ooT
QU/(opt)-110-100-010	2108.12 / ooT	ooT / ooT

- TL-2: 2370.23 sec, (Promising: 13.72 sec)

The results show that the Promising model scales much better than Flat for the tested examples. However, we believe, we may further improve performance significantly over the current results by studying existing model checking techniques. For instance, for certain litmus tests Promising does not perform as well as Flat: tests with a large number of writes whose interleaving does not matter. In such tests, PROMISING explores all interleavings of the writes, and each interleaving leads to a different memory state, even if the order of some writes does not affect the possible final outcomes. Here we believe partial-order reduction techniques [21] can help improve performance.

Where data is available, the results also show the Promising model performs much better than herd. The comparison here is less clear: on the one hand herd does not accurately capture the full ISA behaviour, meaning it has to do less work during the exhaustive search; on the other hand herd is not designed primarily to be a fast model checker, and it is not clear how the axiomatic approach compares to ours in search complexity. Herd computes the set of allowed behaviours in two steps: first, herd enumerates the set of all possible *candidate executions*, concrete executions given by a program-order unfolding, write values for the reads, and relations capturing the concurrency behaviour satisfying only minimal well-formedness conditions; then, herd discards executions violating the model’s axioms. A naive generation of the set of candidate executions is expensive. However, it may be possible to efficiently generate candidate executions using an approach similar to the promise-first enumeration described here, or adapt the model checker of Kokologiannakis et al. [30] based on axiomatic models to ARMv8/RISC-V.

9 Related Work

Models The reference axiomatic memory model, written in herd, and the Flat model have already been discussed. We build on extensive past research on ARMv8 and Power concurrency [6, 7, 10, 11, 18, 19, 22–24, 34, 35, 39–41]. The main inspiration for PROMISING-ARM is the promising semantics of Kang et al. for C/C++ 11 [29]. As described in the introduction, PROMISING-ARM uses the same concepts: views, promises, and certification, but leverages them in a different way: (1) Views consist of a single timestamp, and timestamps at different locations are comparable, reflecting multicopy atomicity. Messages do not carry views, and barriers work purely thread-locally. (2) In order to capture the semantic dependencies, Promising C11 uses *future-memory quantification* for certification, which makes exhaustive execution hard. Here, dependencies are purely syntactic, captured by associating timestamps to registers. (3) The key property of write-first execution (Theorem 7.1) does not hold for Promising C11. The I²E models [14, 43, 44] aim to provide simple models in which instructions execute in order and atomically. However, I²E does not allow load-store reordering, allowed in ARMv8/RISC-V.

Model Checking As demonstrated, our tool can be used for exhaustive state exploration for small instances of concurrency libraries for ARMv8/RISC-V. Since the tool is *sound and complete*, listing precisely the architecturally allowed behaviours, checking such small instances can already be a useful tool for checking the library code: providing confidence in the correctness without generating false positives.

There are a number of existing concurrency model checking tools, none of which, however, apply to ARMv8 or RISC-V. Alglave et al. [8] develop a model checking tool based on axiomatic models for some weaker models including RMO and Power, but not ARMv8, and it does not integrate a substantial ISA model. Abdulla et al. [3–5] describe efficient model-checking algorithms for hardware models (TSO, PSO, and Power), proved sound for Power. They do not handle ARMv8; for their Nidhugg tool, ARM support is called “partial”, under-approximating the behaviours [1], and they do not handle a (Power or ARM) ISA model, but a simple calculus. CDSChecker [37] tackles model checking for a variant of C/C++ 11 that allows load buffering. Kokologiannakis et al. [30] develop an efficient algorithm for a variant of C/C++ 11 that forbids load buffering.

10 Conclusion and Future Work

We have presented an operational model for ARMv8 and RISC-V concurrency, in a different style from the existing ones. The model applies the concepts of promises and views from the Promising C11 semantics to hardware concurrency, to enable a simpler and more abstract operational model. PROMISING-ARM/RISC-V offers the attractive mental model of instructions executing incrementally, instantaneously, and

mostly in program order, which we hope can make the subtle concurrency behaviour of ARMv8 and RISC-V more accessible to both researchers and programmers.

The model enables an executable tool for exhaustive checking and interactive debugging. The experimental results show significant performance improvements over the Flat and herd models in exhaustive search. In the future we plan more work on this – exploring improvements enabled by the model’s abstractness and by applying known model checking techniques. We believe PROMISING-ARM/RISC-V can serve as a basis for other research on hardware concurrency, for formal reasoning about ARMv8/RISC-V concurrent software and for testing and analysis tools.

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